

Industry Standard Architecture (ISA) bus

The original PC expansion bus supported an 8-bit data path (ISA) but the bus was soon extended to support the full 16-bit bus (EISA). Despite the emergence of PCI as an enhanced bus standard, many ISA and EISA cards are still in current use in control and instrumentation systems and are still available from a number of suppliers.

The 62-way ISA (PC expansion bus) connector

The 62-way ISA expansion bus connector was based on a number of direct edge connectors fitted to the system motherboard. One side of the connector is referred to as A (lines as numbered A1 to A31) while the other is referred to as B (lines are numbered B1 to B31). The address and data bus lines are grouped together on the A-side of the connector while the control bus and power rails occupy the B-side.

The following table describes each of the signals present on the 62-way ISA expansion bus connector:

<i>Pin number</i>	<i>Abbreviation</i>	<i>Direction</i>	<i>Signal</i>	<i>Function</i>
A1	/IOCHK	I	I/O channel check	Taken low to indicate a parity error in a memory or I/O device
A2	D7	I/O	Data 7	Data bus line
A3	D6	I/O	Data 6	Data bus line
A4	D5	I/O	Data 5	Data bus line
A5	D4	I/O	Data 4	Data bus line
A6	D3	I/O	Data 3	Data bus line
A7	D2	I/O	Data 2	Data bus line
A8	D1	I/O	Data 1	Data bus line
A9	D0	I/O	Data 0	Data bus line
A10	/IOCHRDY	I	I/O channel ready	Pulsed low by a slow memory or I/O device to signal that it is not ready for data transfer
A11	AEN	O	Address enable	Issued by the DMA controller to indicate that a DMA cycle is in progress. Disables port I/O during a DMA operation in which /IOR and /IOW may be asserted
A12	A19	I/O	Address 12	Address bus line
A13	A18	I/O	Address 13	Address bus line
A14	A17	I/O	Address 14	Address bus line
A15	A16	I/O	Address 15	Address bus line
A16	A15	I/O	Address 16	Address bus line
A17	A14	I/O	Address 17	Address bus line
A18	A13	I/O	Address 18	Address bus line
A19	A12	I/O	Address 19	Address bus line
A20	A11	I/O	Address 20	Address bus line
A21	A10	I/O	Address 21	Address bus line
A22	A9	I/O	Address 22	Address bus line
A23	A8	I/O	Address 23	Address bus line
A24	A7	I/O	Address 24	Address bus line
A25	A6	I/O	Address 25	Address bus line
A26	A5	I/O	Address 26	Address bus line
A27	A4	I/O	Address 27	Address bus line
A28	A3	I/O	Address 28	Address bus line
A29	A2	I/O	Address 29	Address bus line
A30	A1	I/O	Address 30	Address bus line
A31	A0	I/O	Address 31	Address bus line
B1	GND	n.a.	Ground	Ground/common 0V

B2	RESET	O	Reset	When taken high this signal resets all expansion cards
B3	+5V	n.a.	+5V DC	+5V supply voltage
B4	IRQ2	I	Interrupt request level 2	Interrupt request (highest priority)
B5	-5V	n.a.	-5V DC supply	-5V supply voltage
B6	DRQ2	I	Direct memory access request level 2	Taken high when a DMA transfer is required. The signal remains high until the corresponding /DACK line goes low
B7	-12V	n.a.	-12V DC	-12V supply voltage
B8	0WS	I	Zero wait state	Indicates to the processor that the present bus cycle can be completed without any additional wait cycles
B9	+12V	n.a.	+12V DC	+12V supply voltage
B10	GND	n.a.	Ground	Ground/common 0V
B11	/MEMW	O	Memory write	Taken low to signal a memory write operation
B12	/MEMR	O	Memory read	Taken low to signal a memory read operation
B13	/IOW	O	I/O write	Taken low to signal an I/O write operation
B14	/IOR	O	I/O read	Taken low to signal an I/O read operation
B15	/DACK3	O	Direct memory access acknowledge level 3	Taken low to acknowledge a DMA request on the corresponding level (see notes)
B16	DRQ3	I	Direct memory access request level 3	Taken high when a DMA transfer is required. The signal remains high until the corresponding /DACK line goes low
B17	/DACK1	O	Direct memory access acknowledge level 1	Taken low to acknowledge a DMA request on the corresponding level (see notes)
B18	DRQ1	I	Direct memory access request level 1	Taken high when a DMA transfer is required. The signal remains high until the corresponding /DACK line goes low
B19	/DACK0	O	Direct memory access acknowledge level 0	Taken low to acknowledge a DMA request on the corresponding level (see notes)
B20	CLK4	O	4.77MHz clock	Processor clock divided by 3 with 210ns period and 33% duty cycle
B21	IRQ7	I	Interrupt request level 7	Asserted by an I/O device when it requires service (see note)
B22	IRQ6	I	Interrupt request level 6	Asserted by an I/O device when it requires service (see note)
B23	IRQ5	I	Interrupt request level 5	Asserted by an I/O device when it requires service (see note)
B24	IRQ4	I	Interrupt request level 4	Asserted by an I/O device when it requires service (see note)
B25	IRQ3	I	Interrupt request level 3	Asserted by an I/O device when it requires service (see note)
B26	/DACK2	O	Direct memory access acknowledge level 2	Taken low to acknowledge a DMA request on the corresponding level (see notes)
B27	TC	O	Terminal count	Pulse high to indicate that a DMA transfer terminal count has been reached
B28	ALE	O	Address latch enable	A falling edge indicates that the address latch is to be enabled. The signal is taken high during DMA transfers
B20	+5V	n.a.	+5V DC	+5V supply voltage
B30	OSC	O	14.31818MHz clock	Fast clock with 70ns period and 50% duty cycle
B31	GND	n.a.	Ground	Ground/common 0V

Notes:

- 1 Signal directions are quoted relative to the system motherboard; I represents input, O represents output, and I/O represents a bidirectional signal used both for input and also for output (n.a. indicates 'not applicable').
- 2 IRQ4, IRQ6 and IRQ7 are generated by the motherboard serial, disk and parallel interfaces, respectively.
- 3 DACK0 (sometimes labeled REFRESH) is used to refresh dynamic memory while DACK1 to DACK3 are used to acknowledge other DMA requests.
- 4 A / indicates a signal line that is active low (or asserted low).

The 36-way EISA (PC-AT expansion bus) connector

The PC-AT is fitted with an additional expansion bus connector which provides access to the upper eight data lines, D8 to D15, as well as further control bus lines. The AT-bus employs an additional 36-way direct edge-type connector. One side of the connector is referred to as C (lines are numbered C1 to C18) whilst the other is referred to as D (lines are numbered D1 to D18), as shown in Figure 2.3. The upper eight data bus lines and latched upper address lines are grouped together on the C-side of the connector (together with memory read and write lines) while additional interrupt request, DMA request, and DMA acknowledge lines occupy the D-side.

The following table describes each of the signals present on the 32-way EISA expansion bus connector:

<i>Pin number</i>	<i>Abbreviation</i>	<i>Direction</i>	<i>Signal</i>	<i>Function</i>
C1	SBHE	I/O	System bus high enable	When asserted this signal indicates that the high byte (D8 to D15) is present on the data bus
C2	LA23	I/O	Latched address 23	Address bus line
C3	LA22	I/O	Latched address 22	Address bus line
C4	LA21	I/O	Latched address 21	Address bus line
C5	LA20	I/O	Latched address 20	Address bus line
C6	LA19	I/O	Latched address 19	Address bus line
C7	LA18	I/O	Latched address 18	Address bus line
C8	LA17	I/O	Latched address 17	Address bus line
C9	/MEMW	I/O	Memory write	Taken low to signal a memory write operation
C10	/MEMR	I/O	Memory read	Taken low to signal a memory read operation
C11	D8	I/O	Data 8	Data bus line
C12	D9	I/O	Data 9	Data bus line
C13	D10	I/O	Data 10	Data bus line
C14	D11	I/O	Data 11	Data bus line
C15	D12	I/O	Data 12	Data bus line
C16	D13	I/O	Data 13	Data bus line
C17	D14	I/O	Data 14	Data bus line
C18	D15	I/O	Data 15	Data bus line
D1	/MEMCS16	I	Memory chip select 16	Taken low to indicate that the current data transfer is a 16-bit (single wait state) memory operation
D2	/IOCS16	I	I/O chip select 16	Taken low to indicate that the current data transfer is a 16-bit (single wait state) I/O operation
D3	IRQ10	I	Interrupt request level 10	Asserted by an I/O device when it requires service
D4	IRQ11	I	Interrupt request level 11	Asserted by an I/O device when it requires service

D5	IRQ12	I	Interrupt request level 12	Asserted by an I/O device when it requires service
D6	IRQ13	I	Interrupt request level 10	Asserted by an I/O device when it requires service
D7	IRQ14	I	Interrupt request level 10	Asserted by an I/O device when it requires service
D8	/DACK0	O	Direct memory access acknowledge level 0	Taken low to acknowledge a DMA request on the corresponding level
D9	DRQ0	I	Direct memory access request level 0	Taken high when a DMA transfer is required. The signal remains high until the corresponding DACK line goes low
D10	/DACK5	O	Direct memory access acknowledge level 5	Taken low to acknowledge a DMA request on the corresponding level
D11	DRQ5	I	Direct memory access request level 5	Taken high when a DMA transfer is required. The signal remains high until the corresponding DACK line goes low
D12	/DACK6	O	Direct memory access acknowledge level 6	Taken low to acknowledge a DMA request on the corresponding level
D13	DRQ6	I	Direct memory access request level 6	Taken high when a DMA transfer is required. The signal remains high until the corresponding DACK line goes low
D14	/DACK7	O	Direct memory access acknowledge level 7	Taken low to acknowledge a DMA request on the corresponding level
D15	DRQ7	I	Direct memory access request level 7	Taken high when a DMA transfer is required. The signal remains high until the corresponding DACK line goes low
D16	+5V	n.a.	+5V DC	+5V supply voltage
D17	/MASTER	I	Master	Taken low by the I/O processor when controlling the system address, data and control bus lines
D18	GND	n.a.	Ground	Ground/common 0V

Electrical characteristics

All of the signals lines present on the expansion connector(s) are TTL compatible. In the case of output signals from the system mother board, the maximum loading imposed by an expansion card adapter should be limited to no more than two low-power (LS) TTL devices. The following expansion bus lines are open-collector: /MEMCSI6, /IOCS16 and 0WS. Note that the “/” indicates that the signal in question is *active low* (or *asserted low*).

The /IOCHRDY line is available for interfacing slow memory or I/O devices. Normal processor generated read and write cycles use four clock (CLK) cycles per byte transferred. The standard PC clock frequency of 4.77MHz results in a single clock cycle of 210ns. Thus each processor read or write cycle requires 840ns at the standard clock rate. DMA transfers, I/O read and write cycles, on the other hand, require five clock cycles (1050µs). When the /IOCHRDY line is asserted, the processor machine cycle is extended for an integral number of clock cycles.

Finally, when an I/O processor wishes to take control of the bus, it must assert the /MASTER line. This signal should not be asserted for more than 15µs as it may otherwise impair the refreshing of system memory.