

Peripheral Component Interconnect (PCI) bus

The Peripheral Component Interface 'PCI' Bus was originally developed as a local bus expansion for the ISA/EISA (PC/AT) bus. The first version of the PCI bus ran at 33MHz with a 32-bit bus (133MBps) but the current version runs at 66MHz with a 64-bit bus. The PCI bus operates either synchronously or asynchronously with the motherboard clock rate. While operating asynchronously the bus will operate at any frequency up to the maximum (66MHz). Flow control is used to allow the bus to operate with slower devices. The bus is un-terminated and the bus clock operates at 133MHz.

PCI supports full device *bus mastering*, and provides *bus arbitration* facilities through the system chipset. PCI architecture allows bus mastering of multiple devices on the bus simultaneously, with the arbitration circuitry working to ensure that no device on the bus (including the processor) locks out any other device. However, in the event that no other device requires access to the bus, PCI will allow a bus master to transfer data at the maximum permissible rate. Note that, with some early motherboards it might be possible that not all of the available PCI bus slots will be capable of bus mastering. When in doubt it is wise to check with the motherboard manual.

The PCI standard forms part of the *Plug and Play* standard developed by Intel, Microsoft and many other companies in which the *PCI chipset* handles the identification of cards, working in conjunction with the BIOS and operating to automatically allocate resources for compatible peripheral cards.

The PCI bus uses its own internal interrupt system for dealing with requests from the cards on the bus. These interrupts are often called "#A", "#B", "#C" and "#D" to avoid confusion with the normal numbered system IRQs, though they are sometimes referred to by number.

PCI interrupts are mapped to the normal system interrupts (usually IRQ9 to IRQ12). This imposes a limit of four interrupts available for PCI devices. Where more slots are provided (or where a USB controller is present) several PCI devices may be configured to share an IRQ.

Other variants and extensions of the basic PCI specification include:

PCI-X	The latest version 64 bits at 133MHz
cPCI	Compact PCI is PCI in a VME form factor, using either 3U/6U modules and using 2mm connectors
PC/104-Plus	PCI add-on to the PC/104 specification
PISA	PCI add-on for the PC/AT bus standard
P2CI	PCI on the VME64 P2 connector
PMC	PCI on a Mezzanine Card, 'PMC'
PXI	cPCI for Instrumentation
IPCI	Industrial PCI (another version of cPCI)
Serial PCI	PCI based on a serial link
Card Bus	32 bit PCI on the PC Card (PCMCIA) format

The pin connections and signals present on the PCI bus connector are summarised in the following table:

The PCI expansion bus connector

Pin	Name	Description	Pin	Name	Description
A1	TRST	Test Logic Reset	B1	-12V	-12V DC
A2	+12V	+12V DC	B2	TCK	Test Clock
A3	TMS	Test Mode Select	B3	GND	Ground
A4	TDI	Test Data Input	B4	TDO	Test Data Output
A5	+5V	+5V DC	B5	+5V	+5V DC
A6	INTA	Interrupt A	B6	+5V	+5V DC
A7	INTC	Interrupt C	B7	INTB	Interrupt B
A8	+5V	+5V DC	B8	INTD	Interrupt D
A9		Reserved	B9	PRSENT 1	Present
A10	+5V	Power (+5V or +3.3V)	B10		Reserved
A11		Reserved	B11	PRSENT 2	Present
A12	GND03	Ground or Keyway for 3.3V/universal cards	B12	GND	Ground or Keyway for 3.3V/universal cards
A13	GND05	Ground or Keyway for 3.3V/universal cards	B13	GND	Ground or Open (Key) for 3.3V/universal cards
A14	3.3V aux		B14	RES	Reserved
A15	RESET	Reset	B15	GND	Ground
A16	+5V	Power (+5V or +3.3V)	B16	CLK	Clock
A17	GNT	Grant PCI use	B17	GND	Ground
A18	GND08	Ground	B18	REQ	Request
A19	PME#	Power Management Event	B19	+5V	Power (+5V or +3.3V)
A20	AD30	Address/Data 30	B20	AD31	Address/Data 31
A21	+3.3V01	+3.3V DC	B21	AD29	Address/Data 29
A22	AD28	Address/Data 28	B22	GND	Ground
A23	AD26	Address/Data 26	B23	AD27	Address/Data 27
A24	GND10	Ground	B24	AD25	Address/Data 25
A25	AD24	Address/Data 24	B25	+3.3V	+3.3VDC
A26	IDSEL	Initialization Device Select	B26	C/BE3	Command, Byte Enable 3
A27	+3.3V03	+3.3V DC	B27	AD23	Address/Data 23
A28	AD22	Address/Data 22	B28	GND	Ground
A29	AD20	Address/Data 20	B29	AD21	Address/Data 21
A30	GND12	Ground	B30	AD19	Address/Data 19
A31	AD18	Address/Data 18	B31	+3.3V	+3.3V DC
A32	AD16	Address/Data 16	B32	AD17	Address/Data 17
A33	+3.3V05	+3.3V DC	B33	C/BE2	Command, Byte Enable 2
A34	FRAME	Address or Data phase	B34	GND13	Ground
A35	GND14	Ground	B35	IRDY#	Initiator Ready
A36	TRDY#	Target Ready	B36	+3.3V0 6	+3.3V DC
A37	GND15	Ground	B37	DEVSE L	Device Select
A38	STOP	Stop Transfer Cycle	B38	GND16	Ground
A39	+3.3V07	+3.3V DC	B39	LOCK#	Lock bus
A40	----	Reserved	B40	PERR#	Parity Error
A41	----	Reserved	B41	+3.3V0 8	+3.3V DC
A42	GND17	Ground	B42	SERR#	System Error
A43	PAR	Parity	B43	+3.3V0 9	+3.3V DC
A44	AD15	Address/Data 15	B44	C/BE1	Command, Byte Enable 1

A45	+3.3V10	+3.3V DC		B45	AD14	Address/Data 14
A46	AD13	Address/Data 13		B46	GND18	Ground
A47	AD11	Address/Data 11		B47	AD12	Address/Data 12
A48	GND19	Ground		B48	AD10	Address/Data 10
A49	AD9	Address/Data 9		B49	GND20	Ground
A50	Keyway	Open or Ground for 3.3V cards		B50	Keyway	Open or Ground for 3.3V cards
A51	Keyway	Open or Ground for 3.3V cards		B51	Keyway	Open or Ground for 3.3V cards
A52	C/BE0	Command, Byte Enable 0		B52	AD8	Address/Data 8
A53	+3.3V11	+3.3V DC		B53	AD7	Address/Data 7
A54	AD6	Address/Data 6		B54	+3.3V1 2	+3.3V DC
A55	AD4	Address/Data 4		B55	AD5	Address/Data 5
A56	GND21	Ground		B56	AD3	Address/Data 3
A57	AD2	Address/Data 2		B57	GND22	Ground
A58	AD0	Address/Data 0		B58	AD1	Address/Data 1
A59	+5V	Power (+5V or +3.3V)		B59	VCC08	Power (+5V or +3.3V)
A60	REQ64	Request 64 bit		B60	ACK64	Acknowledge 64 bit
A61	VCC11	+5V DC		B61	VCC10	+5V DC
A62	VCC13	+5V DC		B62	VCC12	+5V DC
			64-bit spacer keyway			
			64-bit spacer keyway			
A63	GND	Ground		B63	RES	Reserved
A64	C/BE[7] #	Command, Byte Enable 7		B64	GND	Ground
A65	C/BE[5] #	Command, Byte Enable 5		B65	C/BE[6] #	Command, Byte Enable 6
A66	+5V	Power (+5V or +3.3V)		B66	C/BE[4] #	Command, Byte Enable 4
A67	PAR64	Parity 64		B67	GND	Ground
A68	AD62	Address/Data 62		B68	AD63	Address/Data 63
A69	GND	Ground		B69	AD61	Address/Data 61
A70	AD60	Address/Data 60		B70	+5V	Power (+5V or +3.3V)
A71	AD58	Address/Data 58		B71	AD59	Address/Data 59
A72	GND	Ground		B72	AD57	Address/Data 57
A73	AD56	Address/Data 56		B73	GND	Ground
A74	AD54	Address/Data 54		B74	AD55	Address/Data 55
A75	+5V	Power (+5V or +3.3V)		B75	AD53	Address/Data 53
A76	AD52	Address/Data 52		B76	GND	Ground
A77	AD50	Address/Data 50		B77	AD51	Address/Data 51
A78	GND	Ground		B78	AD49	Address/Data 49
A79	AD48	Address/Data 48		B79	+5V	Power (+5V or +3.3V)
A80	AD46	Address/Data 46		B80	AD47	Address/Data 47
A81	GND	Ground		B81	AD45	Address/Data 45
A82	AD44	Address/Data 44		B82	GND	Ground
A83	AD42	Address/Data 42		B83	AD43	Address/Data 43
A84	+5V	Power (+5V or +3.3V)		B84	AD41	Address/Data 41
A85	AD40	Address/Data 40		B85	GND	Ground
A86	AD38	Address/Data 38		B86	AD39	Address/Data 39
A87	GND	Ground		B87	AD37	Address/Data 37
A88	AD36	Address/Data 36		B88	+5V	Power (+5V or +3.3V)
A89	AD34	Address/Data 34		B89	AD35	Address/Data 35
A90	GND	Ground		B90	AD33	Address/Data 33
A91	AD32	Address/Data 32		B91	GND	Ground
A92	RES	Reserved		B92	RES	Reserved
A93	GND	Ground		B93	RES	Reserved
A94	RES	Reserved		B94	GND	Ground

Notes:

1. Signals on pins 63 to 94 are only used on 64-bit PCI bus cards.
2. The copper foil side of the card is side A whilst the component side is side B.1
3. A # used after a signal name indicates that the signal in question is active low (or asserted low).
4. The time-multiplexed address and data bus may exist as either 0 to 31 bits (32 bits) or 0 to 63 bits (64 bits) using the 64-bit expansion bus. Both address and data signals use the same bus; addresses followed by data. 32-bit PCI may also use 64-bit addressing by using two address cycles, referred to as Dual Address Cycles (DAC), in which the low order address is sent first. Additional control bits are used when the bus is used in 64-bit mode.
5. The bus connectors are labeled “+5V *or* +3.3V” in the case of +5V systems and “+3.3V” for 3.3V systems. Note that the original PCI standard required that plug-in boards use +5V supplies provided by the PC's motherboard. As the PCI standard evolved, the option was added for a +3.3V power source. Furthermore, the newer PCI 2.3 standard has now made the +5V supply obsolete. This means that many of the most recent PCs can only accept 3.3V or ‘universal’ PCI cards. Contacts on the PCI connector (keyways A12, B12, etc) are used to determine the correct power rail voltages (see Figure 2.2).